A.4: FPGA based VME timing boards for Indus-2 timing system

5-Channel coarse and fine delay generator boards :

VME based 5-channel programmable coarse and fine delay generator board has been developed by Accelerator Controls Team of Radio Frequency Systems & Controls Division of RRCAT and deployed in the timing control system of Indus-2, with the aim to use it with 100 MHz clock, 10 ns resolution.

Injection in Indus-2 is controlled using four injection kickers and one booster extraction kicker magnet (two septum magnets are also there). These have to be triggered at particular delay settings (in the range from ns to μs) after each rising coincidence pulse (coincidence of booster and Indus-2 RF clock frequencies). The board is based on XC3S50-4VQ100 (Xilinx FPGA). Coarse delays are generated within FPGA, whereas, DS1023-50 from Maxim is used for generating fine delays with 0.5 ns resolution on the board. On this board, FPGA is used to implement logic for following:

1. VME bus interfacing (data bus, address bus and controls lines interfacing), and logic to read and write channel count values.
2. Channel address decoding for each programmable channel (5 coarse and 5 fine channels).
3. Logic to implement programmable coarse delay for all the 5 channels (all four kickers k1, k2, k3, k4) and booster extraction kicker.
4. Logic for generating control signals for fine delay IC (DS1023-50).

This card is kept completely customisable, which means that JTAG port is provided on board through which the program of FPGA can be upgraded any time in future, in case any modification is required. Power management of FPGA is also handled on board with all the required power supplies (3.3 V for I/O, 2.5 V for configuration, and 1.2 V for internal core of FPGA) generated on board. Clock to FPGA can also be sourced with various options like:

1. Indus-2 RF clock ~ 505 MHz scaled down (this is done through separate ECL logic on board)
2. Direct booster RF clock ~ 31.6 MHz
3. On board clock of 100 MHz

Presently, the card put in the system works at booster RF clock of 31.6 MHz to provide a coarse delay resolution of ~32 ns, but it can used with Indus-2 RF clock in future without any modification.

FPGA Based Coincidence Clock Board:

Timings for Indus-2 are generated based on Indus-2 RF clock (505.8 MHz) and booster RF clock (31.6 MHz). For proper control of the injection and filling process, co-incidence is to be found between the two.

This board achieves the function of generating the coincidence periods between the two clocks. This board also uses XC3S50-4VQ100 Xilinx FPGA device for implementing the logic for coincidence clock from Indus-2 RF clock. It generates coincidence clock from Indus-2 RF clock and a control pulse for interrupt generator card. This board facilitates three different filling modes viz. single bucket, three symmetrical buckets or multiple buckets in the Indus-2 ring.

For both the boards discussed above, Xilinx based ISE8.1 foundation tool for synthesis and bit file generation, ModelSim6.1 tool for functional simulation and timing verification are used, with all coding done in VHDL language for implementing logic.

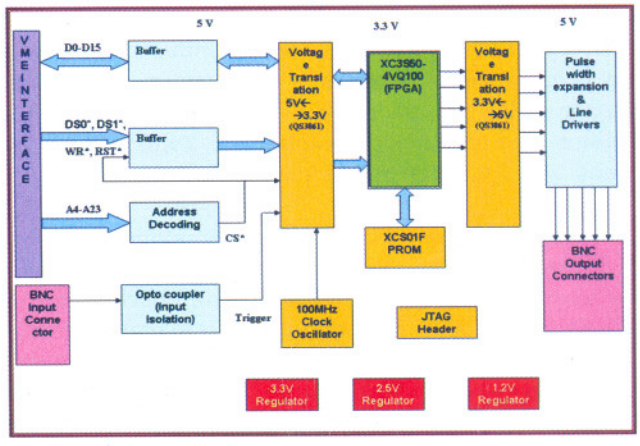

Fig.A.4.1 : Layout of the card.

FPGAs now seem more reliable, customizable and capable than discrete logic ICs to implement even more complex logic with small size (even complex DSP algorithms inside them). In future, more complex functionalities will be incorporated in limited board space like VME while using FPGAs more efficiently.

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