A.7: Development of 1 kW S Band Solid State Driver Amplifier

A 1 kW S Band solid state microwave amplifier has been developed indigenously at PHPMS to drive a 45 MW peak power klystron based microwave system being developed for high energy (30-50 MeV) LINAC and 45 MW S Band accelerator component test facility. This comes as a sequel to the development of solid state microwave amplifiers up to 300 W to drive high power klystrons in RF Systems of 20 MeV pre-injector microtron in INDUS-II complex and10 MeV electron LINAC for agricultural product irradiation. Figure A.7.1 shows the configuration of the amplifier.

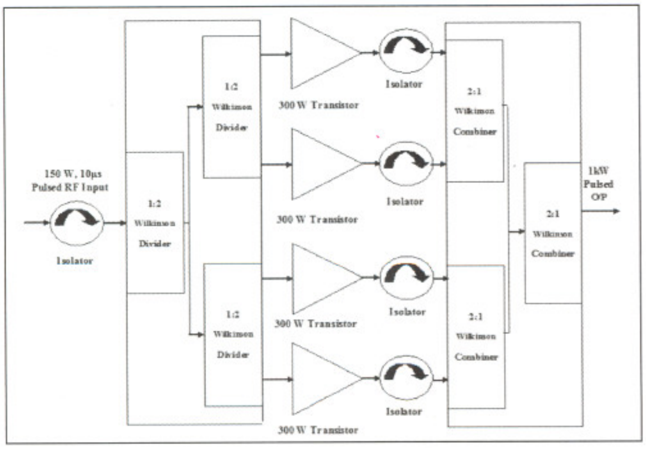

Fig. A.7.1: 1kW S-Band amplifier configuration

The 1kW microwave amplifier has been constructed with four 300 W S Band Class C NPN transistors independently matched to 50 ohms at the input and the output stage. The matching network was been fabricated on a 30 mil thick, low loss substrate of 4.5 dielectric constant. Wilkinson divider and combiners have been used to combine the four amplifiers. In order to ensure better phase match between four ports the combiner/divider has been fabricated using 2.2 dielectric constant 60 mils thick substrate which allows higher dimensional tolerance. The amplifier has been built in three separate stages consisting of divider, transistor amplifier pallet and combiner which have been independently tested before assembling. Table A.7.1 details the test results for combiner/dividers.

Table A.7.1: Measured performance of Wilkinson divider

Parameter	Value
Isolation between output ports	> 24 dB
Amplitude imbalance	± 0.2 dB
Phase Imbalance	± 5 °
Insertion loss	0.5 dB
VSWR	< 1.2

Isolators have been used at the output of each transistor in order to protect it from reverse power. Since connectorised isolators used in previous amplifiers (300 W) were available in the Pulsed High Power Microwave Section (PHPMS), the same has been used in this development. Figure A.7.2 shows the assembled amplifier.

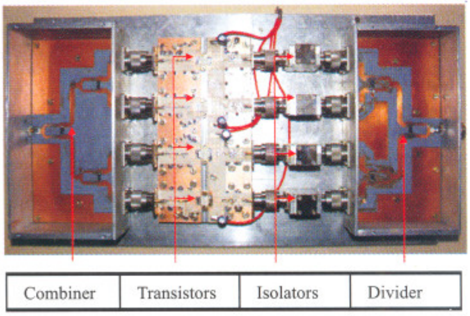

Fig. A.7.2: 1 kW S Band amplifier module assembled with combiner, divider and isolators.

Detailed tests were done on the amplifier to determine its input vs. output curve, frequency response and pulse characteristics. Figure A.7.3 shows the gain response of the amplifier at 40 V operation. Figure A.7.4 shows the pulse shape obtained using a peak power analyzer.

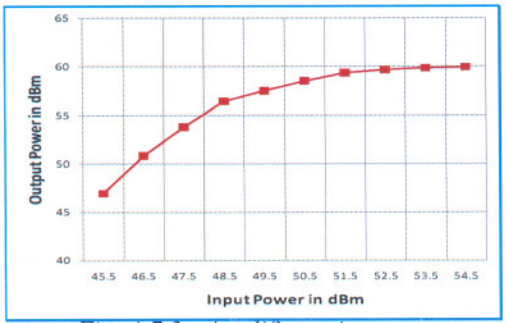

Fig. A.7.3: Amplifier gain response

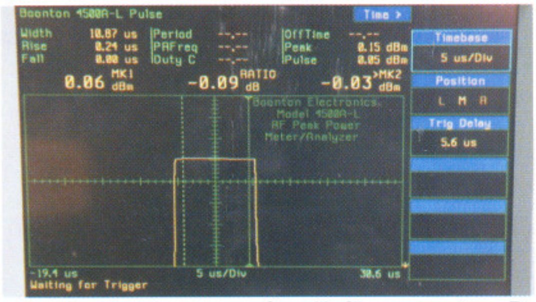

Fig. A.7.4: Output power after 60 dB attenuation. Pulse width 10.5 μs, Amplitude 60.06 dBm

Droop observed is < 0.2 dB for the 10 μs pulse. Variation in output power is within ± 0.1 dB in frequency band 2851 MHz - 2861 MHz.

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