A.4: Design and Development of Digital Low Level RF system

Amplitude and phase stability of RF fields in the accelerating structures are critical for proper injection, acceleration and storage of beam in any particle accelerators. To achieve required stabilities of amplitude and phase in Booster Synchrotron, Indus1 and Indus 2 RF systems of Indus complex, analog based amplitude and phase control loops are used.

Advancement in the field of digital technology has enabled us to develop digital system for RF applications. Digital LLRF system offers inherent advantages like flexibility, adaptability, good repeatability and reduced long term drift errors as compared to analog system. A prototype FPGA based digital LLRF control system employing in phase and quadrature phase (I/Q) scheme has been designed and developed for H-Injector LINAC RF system. A typical Block diagram of Digital LLRF system is shown in Fig. A.4.1.

FPGA based digital LLRF control system

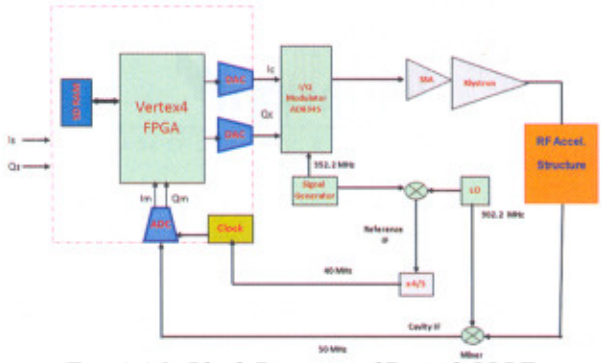

Fig. A.4.1: Block Diagram of Digital LLRF

In this scheme high frequency RF signal (352 MHz) is first down converted to the lower IF frequency (50 MHz) which is achieved by mixing the RF signal with Local Oscillator (LO) operating at 302 MHz.Selection of IF frequency is done considering the bandwidth of RF cavity and clock jitter effects. Synchronization between clock, RF and LO signals is crucial for proper operation of the control loop. RF and LO signals are synchronized using common 10 MHz reference clock.

To detect the amplitude and phase information of IF signal, digital I/Q detection scheme has been adopted. I and Q information is obtained with two consecutive samples by selecting proper sampling frequency. Sampling of IF signal is done at 40 Mega samples per second (MSPS) using 105 MSPS ADC. Digital I/Q detection scheme eliminates the requirement of two separate detectors for amplitude and phase information. Vertex- 4 FPGA based digital controller is designed and developed, which compares the set and detected values of I and Q. Amplitude and phase set values are provided from external PC using RS-232 communication. The control algorithm in FPGA generates control I/Q signal using 105 MSPS DAC. I/Q modulator is used for correcting the amplitude and phase error of the drive RF signal to the amplifier chain. Amplitude and phase of the RF signal at the output of I/Q modulator depends on the control I/ Q signals. This scheme allows us to have common actuator for both amplitude and phase correction.

A prototype digital LLRF system in a 19" test bench was assembled and tested in the lab as shown in the Fig. A.4.2.

Fig. A.4.2: Digital LLRF test bench.

Testing of digital LLRF loop has been successfully done for amplitude and phase correction range of 10dB and 90° respectively by applying the amplitude and phase error as shown in Fig. A.4.3. The amplitude and phase stability better then $\pm$ 1% and $\pm$ 1 degree respectively was achieved.

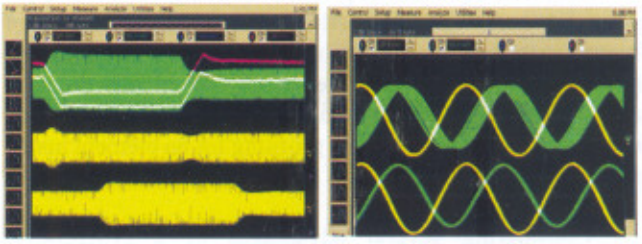

Fig. A.4.3 : Results of amplitude and phase loop correction scheme

Similar scheme will be adopted for different RF systems with minor modifications in hardware and software. Digital LLRF control loop for Indus-2 at 505.8 MHz has also been initiated.

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