A.8: Development of ARM SoC based new dual processor VME CPU board

To replace the old VME CPU boards in Indus-1 and Indus-2 control system hardware and to cater to upcoming new accelerator control system requirements, a new VME32 CPU controller board based on the open source software and hardware concept has been developed. It uses two processors. The first one is ARM Cortex-A53 SoC (System on Chip) on which Linux kernel (version 4.4.15 -v7+) has been ported. The second one is ARM Cortex-M3 on which Free-RTOS (version 8.2.3) has been ported. For both the OS the device driver and Board Support Package (BSP) have been developed, tested and integrated. VME32 interface logic is implemented in FPGA.

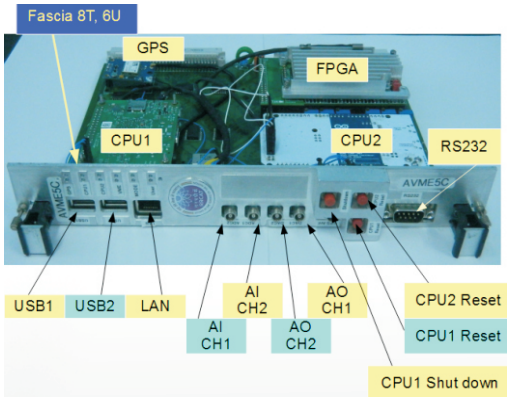

Fig. A.8.1: New VME CPU board interface details.

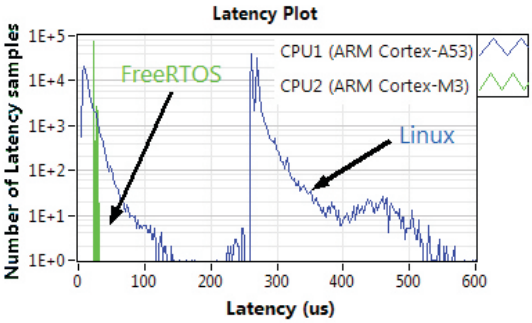

Fig. A.8.2: Measured interrupt latency for LINUX (CPU1) and RTOS (CPU2) on new VME CPU board.

Figure A.8.1 shows different components of this card. Figure A.8.2 shows the interrupt latency for CPU1 (max value ~ 600 s) and CPU2 (max value ~ 32 s). Figure A.8.3 shows different embedded software drivers and FPGA modules and their interconnections. EPICS version R 7.0.1 has been ported on the board and the asynchronous device drivers have been developed. The Command Line interface (CLI) has been developed for both Linux and FreeRTOS for easy development and debugging.

Following are the salient features of the board:

1. VME32: A32/A24/A16/D32/D16/BLT32
2. FPGA: Spartan-6 LX75 (40% free resources)
3. Processors:
   a. CPU1: ARM 64 bit, Quad Core, 1 GHz
   b. CPU2: ARM 32 bit, 84 MHz
4. Memory: 1 GB RAM, 16 GB ROM
5. Inter-CPU communication: Hardware Que, Virtual com port and Streaming Socket, total 27 bidirectional channels are possible.
6. OS ported: Linux, FreeRTOS
7. SCADA ported: EPICS
8. BSP developed for: Linux and FreeRTOS
9. Time sync: GPS, PPS UTC, 40 ns resolution. 1 s accuracy, time stamping at source, cyclic event generation, future time event generation in distributed system environment.
10. Interrupts supported: 05 (VME IRQ 3,4,5,6,7)
11. RTOS measured max latency: ~ 32 s
12. Additional I/O:
    a. 2 Analog Input, 12 bit, 1 Msps
    b. 2Analog outputs, 12 bit, 1 Msps
    c. 4 Status I/O 3.3 V
13. Interface: 2 USB 2.0, 1 LAN 10/100base-T
14. Diagnostics: Readout for +3.3 V, +5 V, +12 V, -12 V, CPU1 Temp, CPU2 Temp, FPGA Temp,
15. 4 Temp measuring devices and 12 status LEDs.

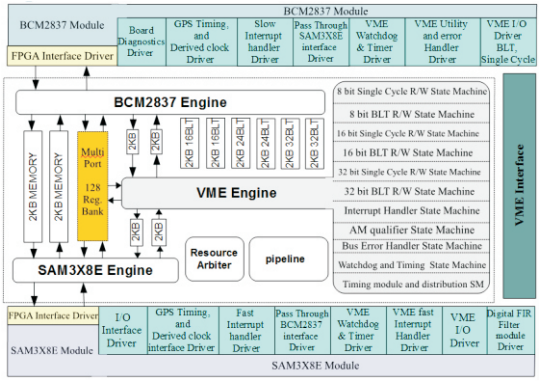

Fig. A.8.3: New VME CPU board software module block diagram and their interconnections.

The card is specifically designed for accelerator control environment (VME I/O + GPS based 40 ns resolution time stamping of events + hard real time performance with RTOS + soft real time performance for SCADA + fast processing on FPGA for feedback control). This card is also of general nature and can be used in almost all the industrial VME SCADA systems.

Reported by:
R. P. Yadav (rpyadav@rrcat.gov.in)