T.3: Advanced harmonically tuned radio frequency power amplifiers

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Abstract

This article addresses design issues for radio frequency power amplifiers with emphasis on emerging design technique of newer harmonically tuned modes, which are superset of conventional tuned load operating modes. It presents a study of the impact of output harmonics and RF transistor's parasitic, on the design of power amplifiers. For high power (~ 500W) designs, increased nonlinearity and dominant device capacitance drastically reduces amplifier efficiency and consequently output power, if they are handled using conventional amplifier operating modes. The fact that hundreds of such modules are required in kW level amplifiers makes it necessary to explore efficient operating modes. Discussion is supported by analysis for calculating proper harmonic terminations by suitable waveform engineering / shaping, resulting in RF efficiency enhancement. In particular, Continuous Class J, Continuous Extended Class F modes with resulting benefits and practical applications are discussed in detail.

1. Introduction

The radio frequency (RF) power amplifiers (PA) are key systems in various commercial [1] and strategic applications [2]. Unparalleled advantages of solid-state technology have made transistor based RF amplifier a promising candidate [3]. Such transistor with moderate power level (~100-800W), appropriately designed with the impedance matching networks and bias circuits, takes the form of a PA module. For achieving hundreds of kW of RF power, multiple PA modules are suitably arranged in multi-stage divide and combine architecture [4], along with power combiner, dividers and directional coupler. As an example, nearly 840 PA modules (each 500 W CW) are deployed in Indus-2 Solid State RF system. For 40 kW, 650 MHz amplifier, designed for horizontal test stand of superconducting cavity, 100 PA modules were used. The potential advantages claimed for high power solid state amplifiers are its long failure-free life, low bias voltage, no risk of x-rays and electric shock, graceful degradation and low projected volume-production costs. In this article focus is on individual PA module and not on the kW level amplifier. Being the main gain block and work horse, PA module determines the system linearity, efficiency and power consumption of the whole system. In order to design it at a high power, the pertaining issues like RF transistor selection, device model, load-line, operating mode and device parasitic effects are important [5]. The biggest challenge in designing harmonically tuned PAs is shaping of the output voltage and current waveforms and realization of RF network to achieve impedance matching simultaneously at fundamental and its harmonics. Majority of the PA design related literature with waveform shaping is available for low power (< 100 W), as its research community [1] is driven by the requirement of communication sector. For a particle accelerator, the required RF signal is mostly monotonic/pulse in nature but RF power requirement is very high (~ > 100 kW) among all applications [6]. In order to fulfill such huge power requirement, this study provides important insights into the evolving landscape of solid state PA along with its design, fabrication and optimization. The cellular phones and base stations require an average RF power of less than 100 W. For this power level, the wave shaping of the voltage waveform at the terminals of the transistor is possible by selecting a device having voltage/current rating higher than the actual requirement. When higher power designs are planned, the optimum calculated values of voltage/current often exceed the maximum rating of the transistor. Adding to this, the large output parasitics of the ubiquitous LDMOS transistor [7] (for UHF PA modules), presents performance related issues unless they are suitably absorbed in impedance matching circuit. Hence, one needs to explore suitable augmentation to newer concept of harmonic tuned design space, so as to apply it for higher power designs.

In the rest of this article, starting from conventional design approach in section 2, newer modes like Class GF, CF, XCF, J and CJ have been discussed. Section 3 gives an overview on the harmonics tuned modes with analytical treatment for voltage current/ waveforms and their associated impedance design space. Practical applications and utility are discussed in section 4.

2. RF PA module design approach

In general, any RF PA design is started with selection of RF transistor. Its selection is enumerated and qualified in terms of its technical features like the power gain, output power, linearity, efficiency, reliability, thermal management, bandwidth, ruggedness and, last but certainly not the least, its cost. At the outset, MOSFETs outperform BJTs for RF amplifier domain. Major issue at high power with the BJTs is a possibility for thermal runaway. This problem is absent in the MOSFET devices because the combined effect of the inversion layer mobility, trans-conductance and the threshold voltage in a MOSFET do not favour for the increase of the drain current with increasing temperature. Among MOSFETs'

families, since early 1990s, the GaN LDMOS [7] has gained wide acceptance for PA applications in VHF to L band. Its topology has the advantage of placing the source terminal at the ground potential, with a geometry layout that improves its thermal performance and minimise its feedback capacitances, and source inductance. Many such advantages translate it into a de-facto device with higher gain, higher power density, and higher DC to RF conversion efficiency for particle accelerator frequency regime.

The schematic of an RF PA is shown in Figure T.3.1. Here, L_{RFC} and C_b are part of biasing network. The drain bias supply voltage is V_{DD}. The PA, performs amplification of this signal, while converting some part of the DC power (P_{DC}) from the bias supply into the RF power (P_1) at the fundamental frequency, delivered through an output matching network. The rest of DC power is dissipated as heat in the transistor and other circuit elements having small but finite resistive and dielectric losses. Such a power conversion mechanism is quantified by the DC to RF conversion or drain efficiency.

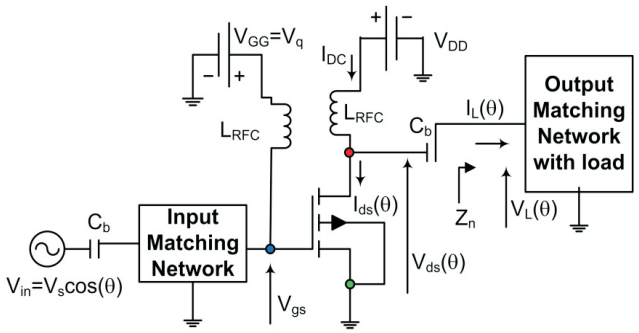

Fig. T.3.1: PA scheme with bias and impedance matching networks.

Assuming steady-state conditions, the time-domain normalised waveforms of voltage and current waveforms at the device output (drain) are expressed as

$$\frac{V_{ds}(\theta)}{V_{DD}} = v_{ds}(\theta) = 1 - \sum_{n=1}^{\infty}[v_n \cos(n\theta + \psi_n)] \quad (1)$$

$$\frac{I_{ds}(\theta)}{I_{DC}} = i_{ds}(\theta) = 1 + \sum_{n=1}^{\infty}[i_n \cdot \cos(n\theta + \xi_n)] \quad (2)$$

where $\theta = 2\pi f_1 t$, and f_1 is the frequency (fundamental) of the RF signal. The drain efficiency is

$$\eta_{pa} = P_1/P_{DC} \quad (3)$$

P_n (RF power at frequency f_n) and P_{DC} are

$$P_n = \frac{V_{DD} \cdot I_{DC}}{2\pi} \int_0^{2\pi} Re(v_1 i_1)\, d\theta \quad (4)$$

$$P_{DC} = V_{DD} \cdot I_{DC} \quad (5)$$

The classical PA design approach, for small signal or low power amplifier, is based on the scattering (S) parameters of the transistor and complex conjugate matching [5]. This approach, based on bias independent linear S parameters, fails as nonlinearity increases.

2.1 Limitation of small-signal design approach

The complex conjugate match is good enough and promises a best possible design for the small signal devices biased for the full cycle conduction of drain current. For high power (>~10W) design, this theory may not suffice due to nonlinear behaviour of the RF transistor at high power, which may change apparent value of device impedance accordingly. It must be noted that the efficiency predicted by this theory is valid if the input drive is sufficient to make full excursion of voltage and current as per transistor's IV characteristics and sufficient harmonic trap is provided in the circuit. Hence, for a large signal PA, a better point to start the design will be the estimation of optimum terminations [8] at fundamental and harmonics, based on the voltage-current waveform engineering and other PA attributes. Each set of such attributes, dealt with operating mode, projects a specific efficiency, linearity, and circuit complexity.

2.2 PA operating modes

Other than waveform engineering, there is a wide choice of operating modes based on different attributes. Such attributes include the bias point selection and matching network topologies (tuned load Class A, AB, B or C) or the operating conditions of the transistor (Class E, Class S, etc.) or harmonic tuning (Class F, CF, XCF, J and CJ etc.). The alphabetical classification of operating modes seems to date back to the earliest era of electronics. Its survival to the present day represents a remarkable continuity, given the vast changes in technology that have taken place in the last few decades. Each set of modes projects a specific efficiency, linearity, input drive power requirement and circuit complexity.

The harmonic shorted version with tuned load (TL), more popularly known as Class A, AB and B modes is based on the identification of the quiescent bias point on VI characteristics of device and current conduction angle (CCA). Among these modes, Class A is most ideal for faithful reproduction of the input RF signal. In fact, a term known as power utilization factor (PUF) is defined as the ratio of fundamental RF output power in operating mode under consideration to the output power obtained in the Class A mode. For these modes, the normalized output (drain) current components, efficiency and power utilization factor (PUF) are shown in Figure T.3.2. As

seen here, the DC current component i_{DC} decreases monotonically as CCA is reduced. For CCA lower than 180°, corresponding to the Class C operation, the DC component continues to drop, but the fundamental component of current also starts to drop below its Class A level. This results in higher efficiency but a lower PUF. These modes, used since decades for low power design, theatrically seem to be quite lucrative. However, once practically materialized, RF performance departs significantly from expected calculated values, specifically for higher power PAs.

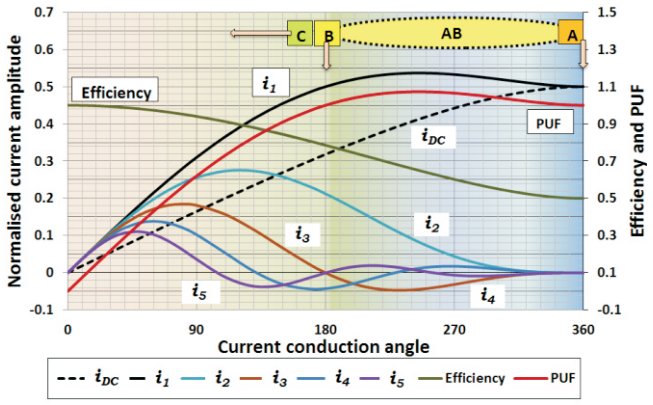

Fig. T.3.2: Normalized current components for tuned load PA operation.

Main reason for the departure from the theory is that the harmonic traps at the load are rarely explicit. Its function is to short-circuit all harmonics other than the fundamental, at the load. In practice, harmonic spectral output powers are below some limit. The output capacitance C_{out} of the device and other parasitic help achieve this trapping. However, for a finite output capacitance the second harmonic component of the voltage is non-zero, and will be not be in phase with the fundamental. This may result in the second harmonic peaking. This reduces the output power and efficiency compared with the ideal (tank circuit) case. With no harmonic trap, the degradation in output power and efficiency can be several decibels. Also the harmonic trap, in a practical circuit, can be provided only for first few harmonics.

In a realistic power LDMOS device, as I_{ds} increases with $V_{gs,}$ device saturation happens at higher and higher drain voltage. This phenomenon gives rise to the knee voltage. It results in a bifurcated I_{ds} when V_{ds} is low. Due to a small but nonzero knee voltage of the transistor, either voltage excursion needs to be reduced or the V_{DD} needs to be increased. In either case, the minima of the voltage waveform is pulled out of the turn-on region. For ideal harmonic shorted case, the fundamental normalized RF output signal delivered to load (denoted by $v_{1,TL}$ for tuned load case) is equal to 1. Due to knee voltage it reduces to 1 - v_k (v_k is normalized knee voltage with respect to V_{DD}) with corresponding reduction in drain efficiency.

The Class D and E or switching-mode of operation is related to the active transistor dynamic operating conditions and consequently to the matching network terminating conditions. The resulting PA could be more properly considered as a DC-to-RF power converter rather than an amplifier, since the input-output transfer characteristics are marginally considered. Such PAs have the potential for high efficiency, with drain efficiency theoretically approaching 100%. However, available power transistors are not ideal switches because of parasitic reactance, finite on-resistance, and limited gain.

3. Harmonically tuned operating modes

For high power design, Harmonic Tuning (HT), has been recent research topic [9] due to the suitable treatment of harmonics, thus contributing to enhancement in fundamental power and efficiency. It is based on the harmonic terminations synthesized across the active transistor, by wave-shaping of output or drain voltage waveform to maximize output power, or efficiency or both. Examples of these classes are the Class GF, Class J, Continuous Class J and Extended Continuous Class F.

The Eq. (1) for drain voltage does generate a rather diverse set of waveforms, depending on the values of the coefficients. The key point is that it should just graze zero value on vertical axis. Instead of zero grazing, if this waveform crosses zero and becomes negative at any point the drain current will drop immediately, resulting in a drastic reduction in the output power and efficiency. Also this current may try to collapse and it may trigger a whole range of highly undesirable effects, like clipping, compression and so on. Such zero-grazing operation, where a relationship can be established between the coefficients causing the voltage waveform to touch but not cross zero, is a necessary condition for all harmonic tuned modes. In harmonic shorted modes, it is implicitly achieved by harmonic traps. For analysis purpose a shifted and normalized version of this waveform is more useful. Eq. (1) may be rearranged as

$$v_{ds,sn}(\theta) = \frac{v_{ds}(\theta)-1}{v_1} = -\sum_{n=1}^{\infty}[k_n \cos(n\theta + \psi_n)] \quad (6)$$

The design coefficients k_n are defined as

$$k_n = v_n/v_1 \quad (7)$$

The design procedure for the harmonic tuned PA includes the optimisation of fundamental component v_1 as a function of design coefficients (k_n and ψ_n); subject to constraints on the

drain voltage excursion. These constraints are dictated by the transistor's physical limits *viz.* V_k (lower limit- knee voltage) and V_{max} (upper limit - max. operating voltage as per transistor's data sheet). As a PA designer, out of two physical limits, the lower one is of a particular interest. For each combination of k_n and ψ_n, the $v_{ds,sn}(\theta)$ is kept above a global minima. Accordingly the lower limit of $v_{ds,sn}(\theta)$ gets translated to $v_{ds,sn}(\theta) \geq -1$. The limiting value of (-1) corresponds to the tuned load operation with fundamental component of drain voltage waveform, equal to $v_{1,TL}$. Taking this value as a reference for HT modes, voltage gain δ *(=* $v_1/v_{1,TL}$*)* occurs when $v_{ds,sn}(\theta)$ takes values greater than (-1) The corresponding $v_{ds,sn}(\theta)$ is a global minimum point derived from $dv_{ds,sn}/d\theta = 0$ condition. Quantitatively the voltage gain is deduced [3] as

$$\delta = -\frac{1}{min[v_{ds,sn}(k_n,\psi_n)]} \tag{8}$$

Comparing to the tuned load operation, an enhancement in the efficiency for harmonic tuned PA with power factor ($\cos\varphi_1$) is given by

$$\eta_{pa,HT} = \delta \cdot \eta_{pa,TL} \cdot \cos(\varphi_1) \tag{9}$$

For simple cases, the calculation of the δ is possible analytically. However, for the higher order HT analysis, the trigonometric complexity escalates rapidly as one solves these equations for the specific coefficients. For such cases, computation can be carried out graphically or by using the factorized expression, as suggested by Cripps [10]. For design purpose, it is necessary to compute a set of positive definite or zero grazing waveform and corresponding impedances for a given current excitation. Figure T.3.3 shows impedance design space and computed efficiency for two simple cases of tuned load modes (Class A, B and AB.), having complex termination at the fundamental frequency, instead of real one (drain voltage expression given in respective Smith chart). The fundamental impedance Z_1 contour, plotted here, sets the diving line between desired (left side) or unclipped and clipped (right side) drain voltage waveforms. The area enclosed by the curves A and B represents the impedances, which can deliver efficiency equal or greater than 50%. For a practical PA design, it should be remembered that these impedances correspond to their values at the current generator plane of the MOSFET. The frequency dependent parasitics, due to the device as well as its package, need to be incorporated before designing matching network at the accessible reference planes of the MOSFET. To determine the continuous optimum load impedances at such physical plane, the large-signal model of the packaged transistor is used in the circuit simulation.

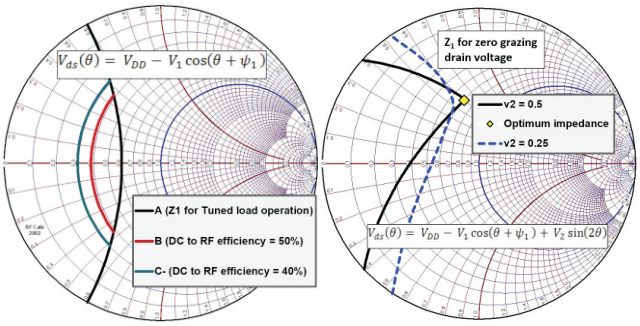

Fig. T.3.3: Design curves plotted on Smith charts for non-zero crossing drain voltage waveforms.

Most of the classical modes and HT modes can be inverted [11], which means that the current and voltage waveforms can be reversed. The inverse Class F PA [12] requires a square current waveform and a half wave rectified sinusoidal waveform at the device intrinsic current generator plane. Interesting cases tackling concurrently both input and output harmonics (Class GF and GF^{-1}) are reported [9] recently.

Pure harmonically terminated operating modes like Class J and Class F requires a high peak voltage at the drain terminal of the transistor ($> 3V_{DD}$). The present device technology for the UHF power MOSFETs, hardly permits this voltage (V_{max}) to be more than twice of the rated power supply voltage (V_{DD}). Other sub optimum solutions to resolve this problem, lies in the selection of angle ψ_1 other than the optimum one. Such solutions present a design space for a given device and its practicalities. The resulting operation modes, from such solutions, are known as *continuous* modes of transistor operation. Unlike low frequency PA, a limited number of harmonics can be effectively controlled in RF and microwave PAs. Also this limit is indirectly imposed by large output shunt capacitance (of the order of 100-200 pF) of UHF power transistors, operating in a power regime of 300-500 W. It provides a short circuit to the higher order harmonics generated at the transistor plane. Also sometimes the benefits achieved by managing the higher-order harmonics become negligible, if they are compared to the growing circuit complexity and the resulting power loss. Thus at RF and microwave, PA design techniques make use of limited harmonic components to result the best possible performance. Some specific cases of HT operation, with third or second harmonics or mixture of these components to drain voltage waveform, are discussed briefly now.

3.1 Third harmonic tuned case and Extended Continuous Class F operation

This Class of PA is based on the idea of finding the proper termination with n = 4 in Eq. (1) for the third harmonic component ($k_3 \neq 0$) only, while assuming the even ones to be short-circuited ($k_2 = k_4 = 0$). The nonlinear output capacitor also helps producing this third harmonic component of the current. It is also assumed that phase shift of individual voltage components are zero ($\psi_n = 0$). Resulting voltage waveform is

$$v_{ds}(\theta) = [1 - v_1\{\cos(\theta) + k_3 \cos(3\theta)\}] \quad (10)$$

It is plotted in Figure T.3.4 for Class B input current excitation, along with its components, third harmonic component $v_{2,HT}$ (v_3 for HT case) and the fundamental part $v_{1,HT,}$ for clarity. For comparison, the tuned load fundamental voltage component $v_{1,TL}$ is also shown. For determining voltage gain in terms of design coefficient, the values of θ where the first derivative of Eq. (6) becomes zero must be identified. Under these constraints, solution of voltage gain [3] gives

$$\delta = -1/\left(\frac{3k_3-1}{3} \cdot \sqrt{\frac{3k_3-1}{3k_3}}\right) \quad (11)$$

It exhibits a maximum value of (2/√3) corresponding to k_3 equal to (-1/6).

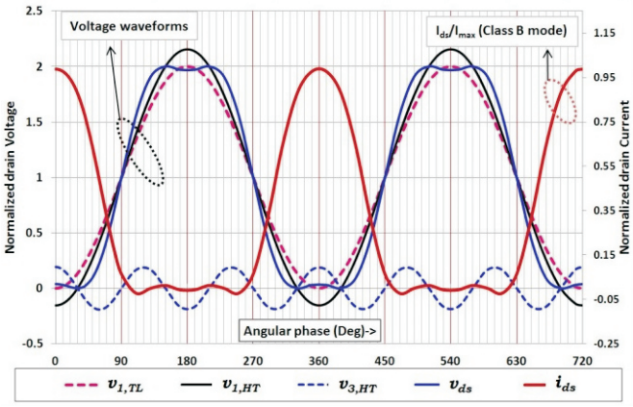

Fig. T.3.4: Drain voltage and current waveforms for third harmonic waveform shaping.

Substituting these values in Eq. (10), we get

$$v_{ds}(\theta) = \left(1 - \frac{2}{\sqrt{3}} \cos\theta + \frac{1}{3\sqrt{3}} \cos 3\theta\right) \quad (12)$$

Also tuned load (Class B) efficiency gets enhanced as

$$\eta_{pa,HT} = \delta \cdot 78.5\ \% = 90.64\%$$

This is an upper limit of the efficiency. The resulting terminations at the current generator plane of the transistor are expressed as

$$Z_1 = \left(\frac{2}{\sqrt{3}}\right) \cdot \frac{V_{DD}}{I_1(\theta)},\ Z_2 = 0,\quad Z_3 = \infty \quad (13)$$

One possible realization for achieving simultaneous fundamental and harmonic matching (2S= Z_2 = 0,3O = Z_3 = ∞) for this case is shown in Figure T.3.5.

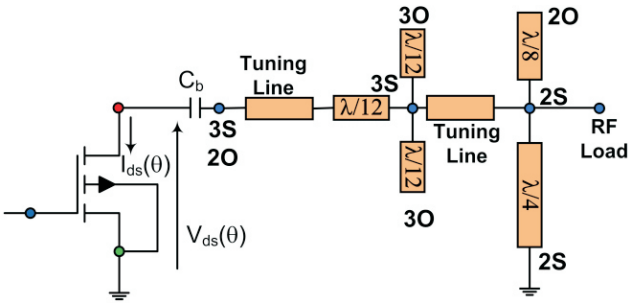

Fig. T.3.5: Possible output matching network for third harmonic tuned case.

From a practical point of view, specifically due to transistor's parasitics, these values of Z_2 and Z_3 at the intrinsic transistor's terminals, pose significant restrictions. Hence, design needs to be explore in suboptimum region by introducing additional design parameters (α, β and γ) For such case mathematical complexity reduces by using Cripps's factored form. Noting that such condition includes a *zero-grazing* double root, Cripps [10] encapsulated this condition by expressing v_{ds} (θ) as

$$v_{ds}(\theta) = (1 - \alpha\cos\theta)^2 \cdot (1 + \beta\cos\theta) \cdot (1 - \gamma\sin\theta) \quad (14)$$

With proper mathematical treatment [3], the optimum value of α and β can be obtained. Using these values Eq. (14) becomes

$$v_{ds}(\theta) = (1 - \frac{2}{\sqrt{3}}\cos\theta)^2 . \left(1 + \frac{1}{\sqrt{3}}\cos\theta\right) . (1 - \gamma\sin\theta) \quad (15)$$

This equation, with α and β parameters as constant and variable γ (-1 ≤ γ ≤ 1) results in Continuous Class F or CF mode of PA operation [12]. The important aspect is that one need not provide an ideal short circuit for the second harmonic. For few specific values of γ IV waveforms are plotted in Figure T.3.6. In general α and β can also be varied, to get an additional degree of freedom for the PA design. Such variations result in Extended Continuous Class F or XCF design space [13]. This mode provides an additional flexibility which can be used to maintain acceptable

fundamental power and DC to RF conversion efficiency, without crossing the voltage breakdown limit V_{max} of the transistor. Hence, this mode of operation seems suitable for high power PA designs with UHF power transistors.

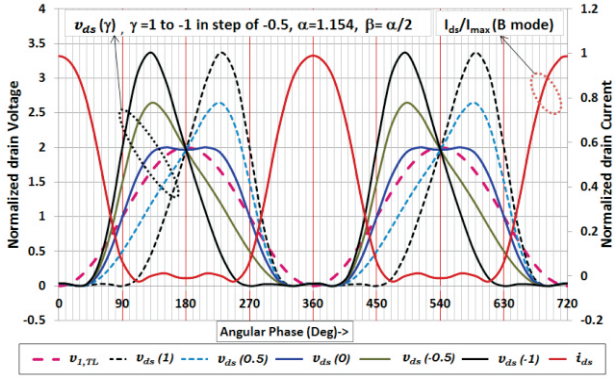

Fig. T.3.6: Drain voltage and current waveforms for Continuous Class F operation.

This design space for high power amplifiers can provide more flexibility for selecting an output matching network so that the resulting device stress for voltage and current can be kept within the safe limit. Obviously, the efficiency will be lower than the maximum value obtained in the CF mode. The XCF design can be performed by selecting suitable values of α, β and γ VI design space is plotted with Class B current excitation, in Figure T.3.7. As seen here, γ manages the phase shift between voltage and current. For the general case, including all the three design space parameters, different terminations for XCF mode can be derived. The fundamental power in this mode is given by

$$P_1 = \left(\alpha - \frac{\beta}{2} - \frac{3\alpha^2\beta}{8}\right) \cdot V_{DD} I_1(\Phi) \qquad (16)$$

where ϕ is current conduction angle.

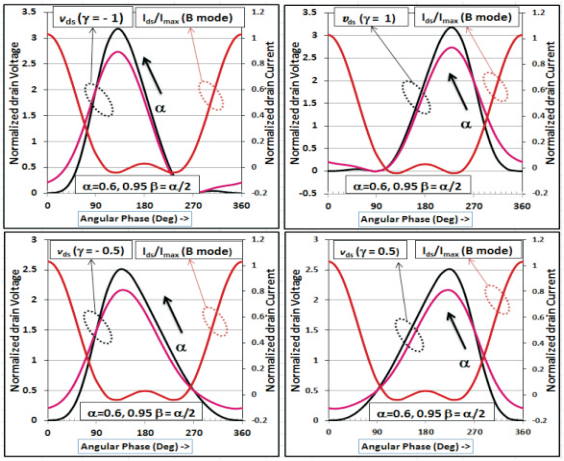

Fig. T.3.7: Different drain voltage waveform for Extended Continuous Class F mode.

3.2 Second harmonic tuned case and Continuous Class J operation

In this mode of operation, necessary measures are taken to control the second harmonic voltage component only, while short-circuiting the other coefficients ($k_3 = k_4 = 0$) Such operating mode was reported in 2009 by Cripps, named as a Class-J mode [14]. As discussed previously for class F mode, pure second harmonic tuned case is difficult to realize for high power transistor. On a similar token, continuous mode of the Class J operation seems suitable for higher power, instead of pure Class J. For such a case the drain-source voltage waveform can be represented in a non-crossing-zero factored expression. Each of the factors in such an expression can never take on a negative value, regardless of the value of θ so

$$v_{ds}(\theta) = (1 + \alpha \sin\theta) \cdot (1 - \beta \cos\theta) \qquad (17)$$

This equation represents a Continuous Class J family of zero-grazing waveforms, which retain the constant fundamental power, as the parameter α is varied from -1 to +1 Figure T.3.8 shows these waveforms, for a single (ideal) value of β. With α equal to zero, this waveform represents the familiar Class B case. The upper limit of α represents the Class J operation whereas the lower limit represents the inverse Class J operation. The value of β is linked with v_k parameter of the transistor. Values of α and β control extrema points of v_{ds} . The peak voltage for each waveform is different and it increases with increasing value of α The design parameters k_2, ψ_1 and ψ_2 are obtained by comparing Eq. (17) with Eq. (1) for n=2 as

$$k_2 = -\frac{\alpha\beta}{2\sqrt{\alpha^2+\beta^2}}, \quad \psi_1 = \tan^{-1}\left(\frac{\alpha}{\beta}\right), \psi_2 = \frac{\pi}{2} \qquad (18)$$
$$\delta = \sqrt{\alpha^2+\beta^2}$$

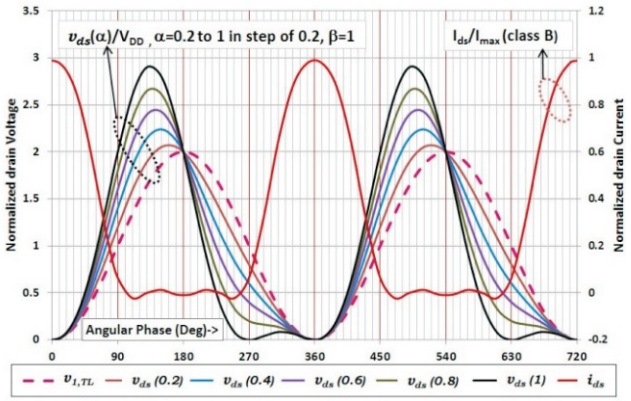

Fig. T.3.8: Drain voltage waveform for different values of and constant value of .

Thus Continuous Class J design space [15] is manageable for design, in terms of α and β. For demonstrating voltage gain achieved, a family of $v_{ds,sn}(\theta)$ is plotted in Figure T.3.9. Here, $v_{1,TL,sn}$ corresponds to the normalized and scaled version of $v_{1,TL}$. Taking the minimum value of $v_{1,TL,sn}$ as a reference, the voltage gain for different waveforms is depicted here. For highlighting this gain, the variation is shown only for a small interval of the angular phase from 180° to 450°.

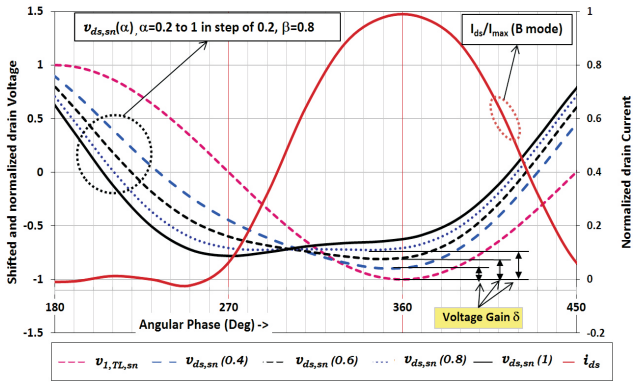

Fig. T.3.9: Shifted and normalized drain voltage waveform for different values of α in CJ mode.

4. Application and utility

In order to verify the theoretical analysis, many PAs were designed, based on developed harmonic tuned concepts, and experimentally tested for various figures of merit. This section describes two most prominent designs which found immediate application in RRCAT projects. The first design is for a Continuous Class J mode PA, operating at a center frequency of 505.8 MHz with output power up to 500 W [15]. The second PA was designed at 650 MHz using Extended Continuous Class F operation, to deliver 600 W [13]. More than 1200 PA modules of first design have been manufactured and successfully deployed in Indus-2 in different 75 kW solid state RF amplifiers [16], over a period of time. Similarly based on second design, more than 100 PA modules have been successfully fabricated and tested as part of 40 kW, 650 MHz solid state amplifier, developed for Horizontal Test Stand and IIFC programme.

4.1 Continuous Class J mode power amplifier

For the Continuous Class-J based PA design, BLF 573 LDMOS transistor was selected on the basis of the load-line calculation and preliminary nonlinear circuit simulation studies. Its typical CW performance at 225 MHz include an average output power of 300 W with a power gain of 27.2 dB and a drain efficiency of 70%; all at a drain supply voltage of 50 V (DC). Hence, in order to achieve the power of 500 W and above, from a single PA, two such transistors were power combined in a single PA with the help of on-board Wilkinson divider and combiner. The fabricated amplifier board (Figure T.3.10.) was mounted on a water-cooled copper plate.

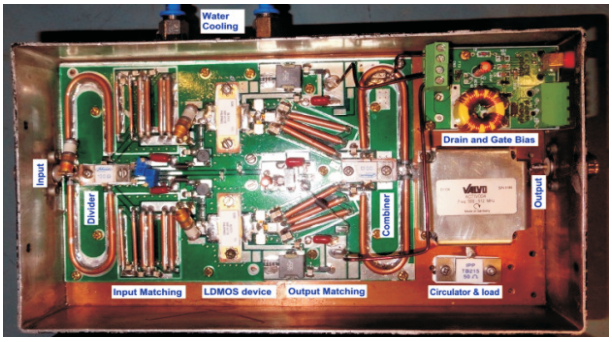

Fig. T.3.10: Fabricated 500 W PA module.

As per the data sheet, the peak voltage at drain terminal for this transistor cannot exceed 110 V. Thus values of α and β need to be calculated [3], so as to keep the maximum drain voltage V_{max} below 2.2 times that of the drain supply of 50 V. Table T.3.1 gives calculated δ, upper and lower limits of the drain voltage, for different α and β. The design set, comprising α=0.5 and β=0.86, (φ_1=30.17°) fulfills the PA requirement with upper (V_{max} =110V) and lower (V_k =7V) limits of drain voltage.

Table T.3.1: Calculated voltage gain, maximum and minimum drain voltages.

Sr.	α	β	δ	V_{max} (V)	V_{min} (V)
1.	0.40	0.80	1.04	101.6	9.9
2.	0.50	0.80	1.16	105.8	9.7
3.	0.50	0.86	1.16	109.0	7.0
4.	0.60	0.80	1.16	110.5	9.5

The nonlinear output capacitor was estimated [3] by

$$C_{out}(V_{ds}) = 50.[1.9 + 1212\{1 + \tanh(-0.0465V_{ds} - 2.7)\}]\ pF \quad (19)$$

The designed PA was fully characterized on a high power RF test bench. The swept power parameters, measured using this test bench, are shown in Figure T.3.11. Since the output power of this PA is quite high, large signal operation was studied with the help of X parameter™ measurement (Figure T.3.12) of this PA. These parameters are based on the Poly-Harmonic Distortion (PHD) approach [17]. Large signal output reflection coefficient $X^{(S)}_{22,11}$ and $X^{(T)}_{22,11}$ refer to large signal output match.

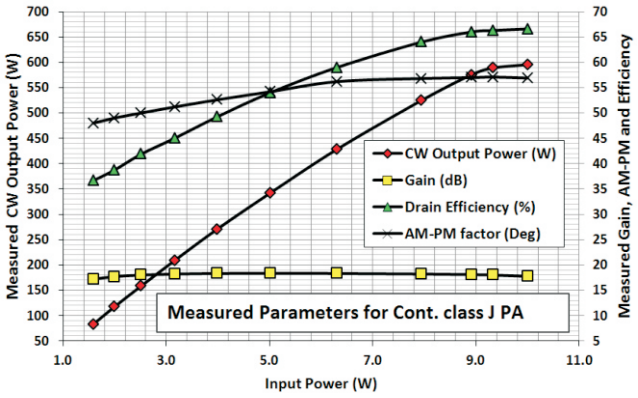

Fig. T.3.11: Measured RF performance of 500 W PA module at 505.8 MHz.

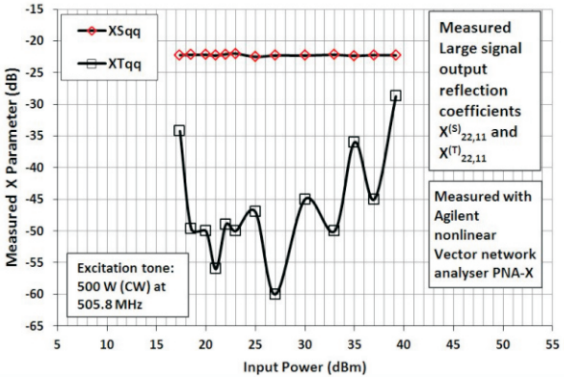

Fig. T.3.12: Measured X parameter for at 500 W.

As seen in this figure, for small as well large input amplitude, the output match is pretty good. $X^{(T)}_{22,11}$ is appreciable only for large-signal (nonlinear) conditions.

4.2 Extended Continuous Class F mode amplifier

Second high power design was carried out at 650 MHz. The design parameters for this PA include a power gain of 19 dB, a bandwidth of 5 MHz and its spurious response below 30 dB from the fundamental signal. Based on the nonlinear circuit simulation studies and these specifications, MRFE6VP8600H transistor was selected. The target efficiency was set at 70% in view of practicalities ($V_k \approx 7V$) of the transistor. A photograph of the fabricated PA is shown in Figure T.3.13.

The measurement [15] for the output power, efficiency and power gain, performed for this PA using the RF test bench, are shown in Figure T.3.14. As seen here, the measured efficiency at the saturate power of 600 W is near 68%, (with output circulator having insertion loss of 0.2 dB) with a power gain of 17.8 dB.

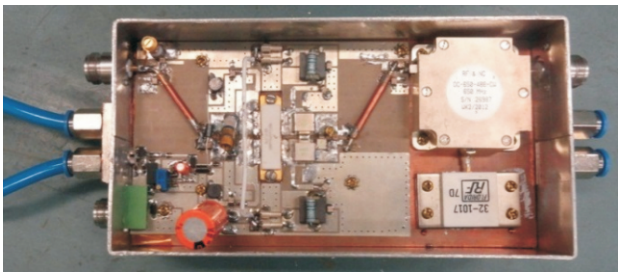

Fig. T.3.13: Fabricated PA in Extended Continuous Class F mode.

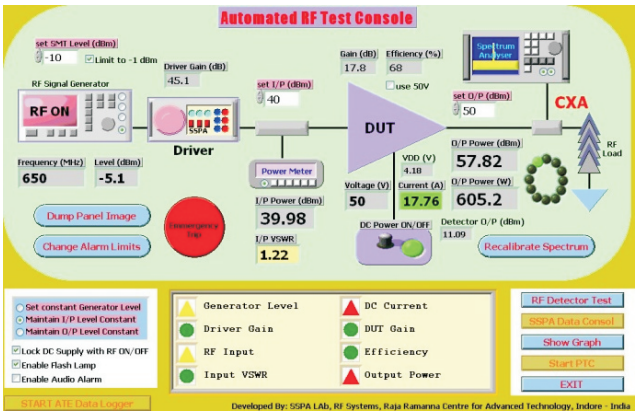

Fig. T.3.14: Measured high power parameters of 650 MHz PA.

5. Summary

In this article, along with discussion on advanced and emerging harmonically tuned operating modes for power amplifiers, two novel variants *viz.* the Continuous Class J and Extended Continuous Class F mode amplifier in 500-700 W power regimes are physically demonstrated. These designs were mass produced and used in Indus-2 RF system and 650 MHz amplifiers, respectively. It is shown that the wide zone of RF power amplifier design, mainly driven by the communication segment, can be narrowed down to cater the requirements of the particle accelerator. Unlike the conventional modes with shorted harmonics at the output, in these modes the output voltage waveform of the PA is engineered and optimized by selecting a set of harmonic terminations, for the given bias and input drive conditions. This approach provides some flexibility in impedance matching in view of transistor's parasitics, specifically for higher power designs. Different theoretical analysis suitably supported by the experimental investigation, presented in this article, seems promising techniques for high power RF amplifier design.

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